AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 4, line 21 with the following rewritten paragraph:

-- As shown in Fig. 1, deep trench capacitors 102 are formed into a matrix and disposed in the substrate 100. Each deep trench capacitor 102 includes a top electrode 102a, an isolation layer 102b, and a storage electrode 102c, and has a vertical transistor 104 disposed thereon. Each vertical transistor 104 includes a gate 104a, a gate oxide layer 104b, a source 104c and a common drain 104d. The gate oxide layer 104b is the sidewall at the bottom of the gate 104a, and the vertical region between the source 104c and the common drain 104d in the substrate 100 is the channel of the transistor 104. In addition, an isolation layer 108 and an ion diffusion layer 106 are disposed between the gate 104a and the top electrode 102a of the deep trench capacitor 102. The sidewall of the isolation ~~layer 106~~ layer 108 is the source 104c, and the isolation layer 108 is disposed between the gate 104a and the ion diffusion layer 106 for electrical insulation.

Please replace the paragraph at page 9, line 4 with the following rewritten paragraph:

-- In the present invention, the test device 200 disposed in the scribe line region and a plurality of memory cells with vertical transistors in the memory region are formed simultaneously. For example, the deep trench capacitors 102 of the memory cells in the memory region and the H-type deep trench capacitor (D_{11}, D_{12} and D_{21}) in the active area A_1 are formed simultaneously with the same masks, process and conditions. The word lines 118a~118b of the memory cells in the memory region and the first to fourth conductive pads P_1~P_4 and the bar-type conductive pad P_{51} are formed simultaneously with the same masks, process and conditions. Therefore, the memory region and the test device may have the same alignment shift between deep trench capacitors (102, D_{11} and D_{12}) and word lines (118a~118d, [[P_1~P_5]] P_1~P_4 and P_{51}) use of the same masks and the same process. Thus, alignment of deep trench capacitors and word lines in memory region can be obtained according to whether the first resistance R_1 equals the second resistance R_2.

Please replace the paragraph at page 10, line 20 with the following rewritten paragraph:

-- The memory region and the test device may have the same alignment shift between deep trench capacitors (102, D_{11} and D_{12}) and word lines (118a~118d, [[P_1~P_5]] $\underline{P_1 \sim P_4}$ and P_{51}) use of the same masks and the same process. Thus, alignment of deep trench capacitors and word lines in memory region can be obtained according to whether the first resistance R_1 equals the second resistance R_2. The alignment shift between deep trench capacitors and word lines in the memory regions can also be obtained according to the equation 4.